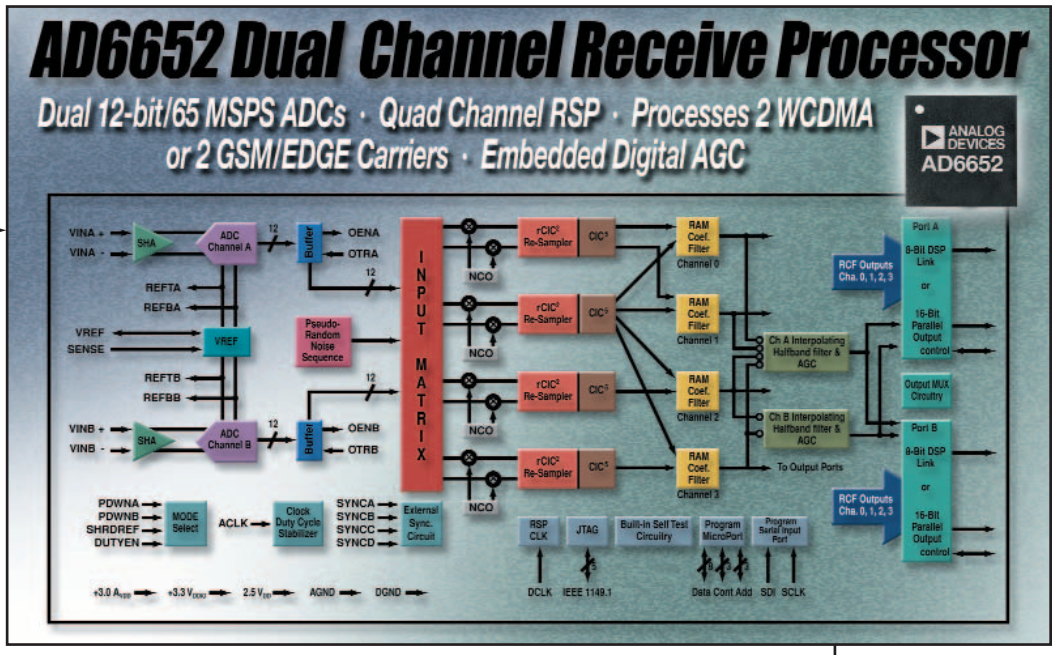
AD6652 IF to Baseband Diversity Receiver



Features

- Integrated 12-bit dual channel ADC
- Sample rates up to 65 MSPS
- IF sampling frequencies to 100 MHz
- SNR = 70 dB (to Nyquist), SFDR = 85 dB (to Nyquist)
- Power-down to <2 mW
- Internal voltage reference
- Internal sample-and-hold analog input
- Flexible analog input (1 V to 2 V p-p)
- Differential or single-ended analog input
- Clock duty cycle stabilizer
- –80 dB channel crosstalk @ f_{IN} = 10 MHz
- Quad channel receive signal processor (RSP)
- Four independent receivers in a single package
- Crossbar switched receive processor inputs
- Digital resampling for noninteger decimation rates
- Programmable decimating FIR filters
- Flexible control for multicarrier and phased array
- 196-lead BGA package
- Member of the VersaCOMM+® family. Visit www.analog.com/VersaCOMM for more information.

Applications

- Communications
- Diversity radio systems
- Multimode digital receivers: GSM, PHS, AMPS, UMTS, WCDMA, CDMA-ONE, IS95, IS136, CDMA2000, EDGE, IMT-2000
- Smart antenna systems
- General-purpose software radios
- Broadband data applications
- Instrumentation and test equipment
- Micro and pico cell systems
- Wireless local loop
- In-building wireless telephony

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High Performance Capabilities for Digital Up/Down Conversion	AD6652
High speed NCO frequency translation	✓
Decimating filters	✓
AGC support	✓
Noninteger data rate resampling	✓
Synchronized operations (hop, ramp, mode)	✓
Programmable filter response	✓
JTAG, BIST, PN generation	✓
Phase equalization	
Digital modulation (GMSK, QPSK, 8PSK)	
Interpolating filters	✓
On-chip ADC	✓
On-chip DAC	

ADC/RSP Integration Advantages

- Embedded high performance IF sampling ADCs
- Uses proven product cores
- Cuts development time and is cost competitive
- Reduces board layout space and complexity
- Reduces component count and interconnect parasitic oscillations
- Enhanced testability and reliability
- RSP channels provide signal processing gain
- Embedded digital AGC in the RSP back end
- 3 V ADC cores and 2.5 V digital cores

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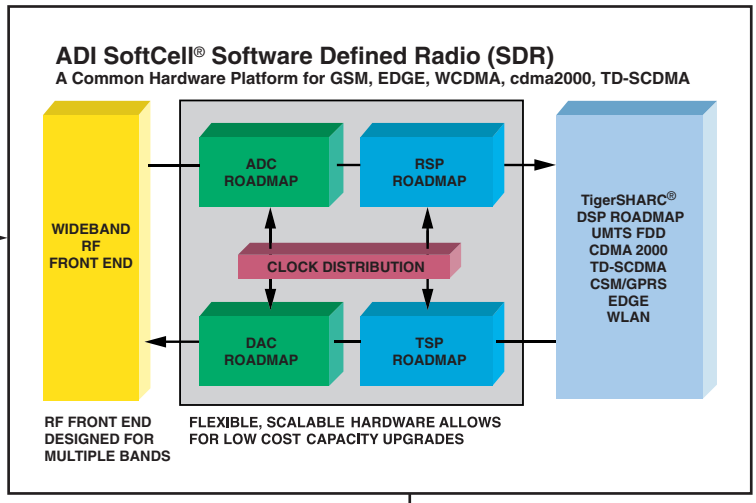

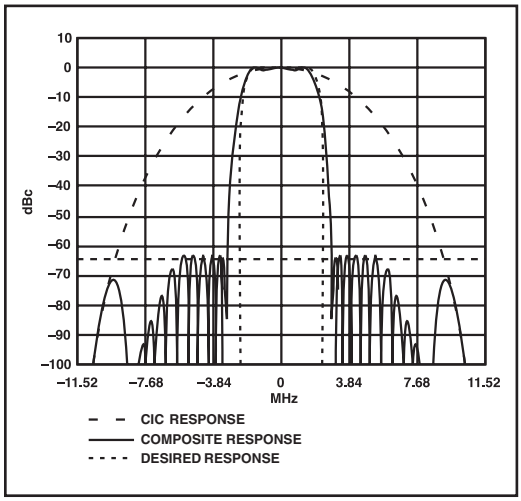

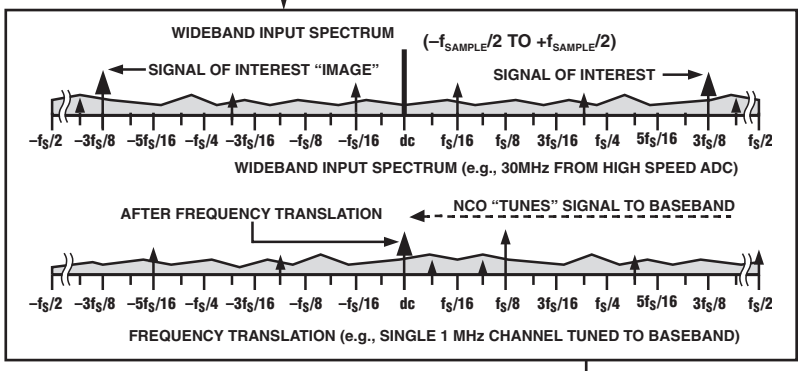
WIDEBAND INPUT SPECTRUM
(–fSAMPLE/2 TO +fSAMPLE/2)
SIGNAL OF INTEREST "IMAGE"
SIGNAL OF INTEREST
–fS/2 –3fS/8 –5fS/16 –fS/4 –3fS/16 –fS/8 –fS/16 dc fS/16 fS/8 3fS/16 fS/4 5fS/16 3fS/8 fS/2
WIDEBAND INPUT SPECTRUM (e.g., 30MHz FROM HIGH SPEED ADC)
AFTER FREQUENCY TRANSLATION
NCO "TUNES" SIGNAL TO BASEBAND
–fS/2 –3fS/8 –5fS/16 –fS/4 –3fS/16 –fS/8 –fS/16 dc fS/16 fS/8 3fS/16 fS/4 5fS/16 3fS/8 fS/2
FREQUENCY TRANSLATION (e.g., SINGLE 1 MHz CHANNEL TUNED TO BASEBAND)

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Printed in the U.S.A.

H03605-.5-3/03(0)

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